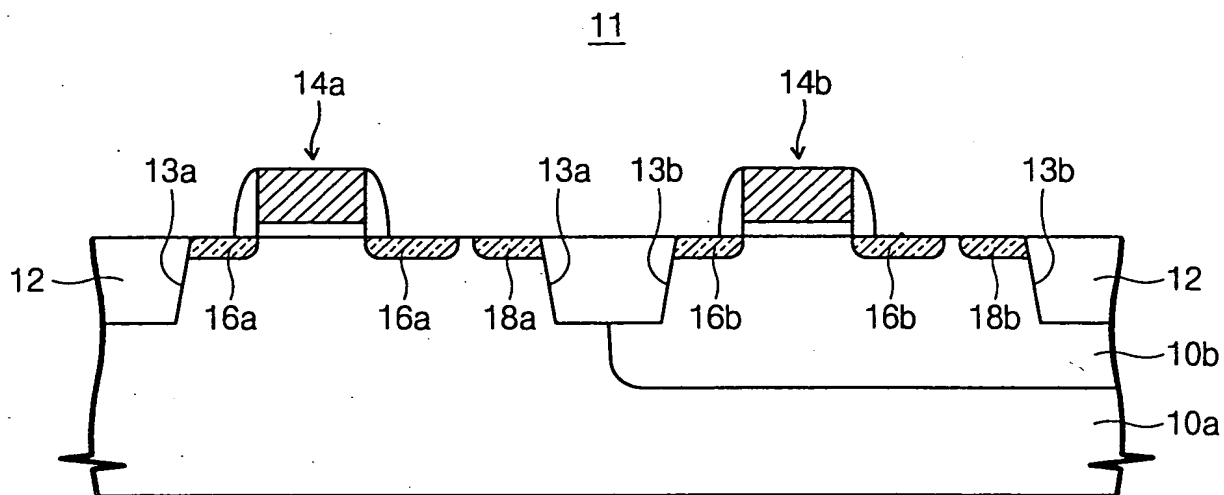


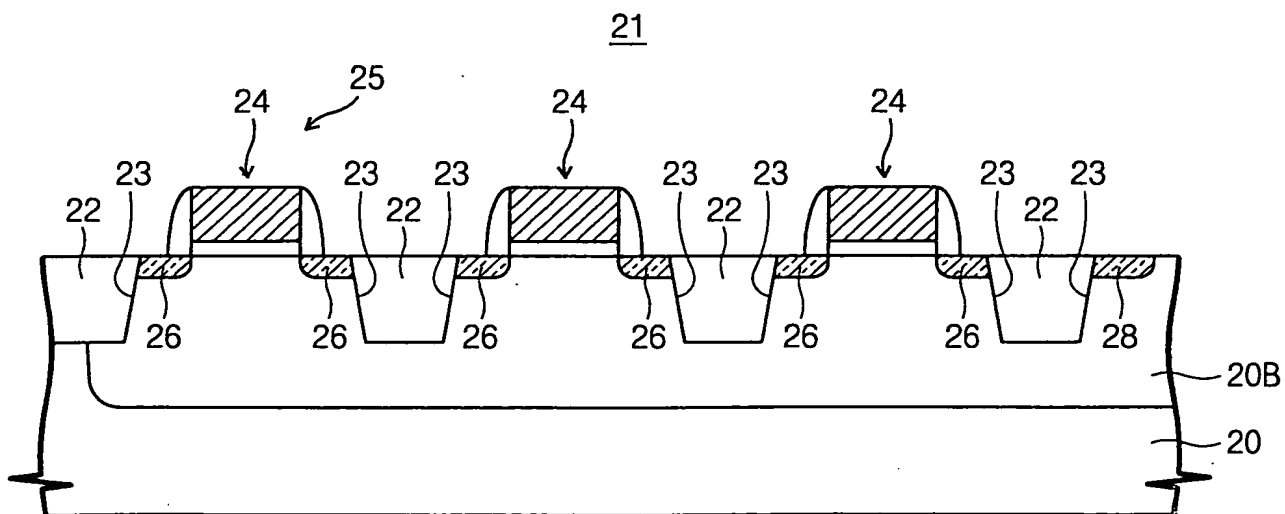
**Fig. 1**

(Prior Art)



**Fig. 2**

(Prior Art)



3  
Fi.

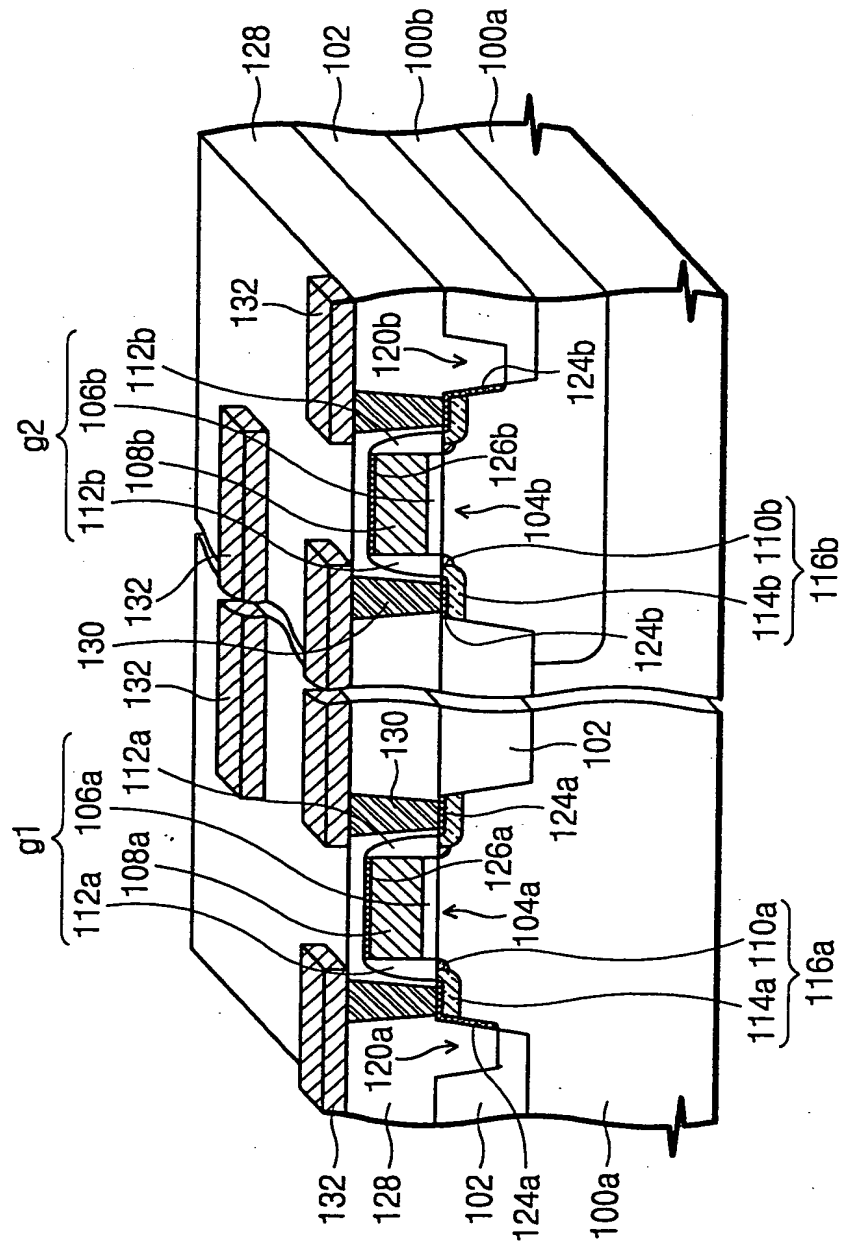


Fig. 4

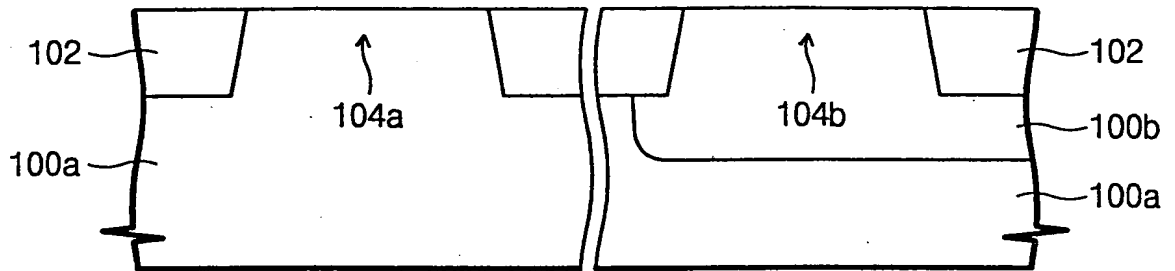
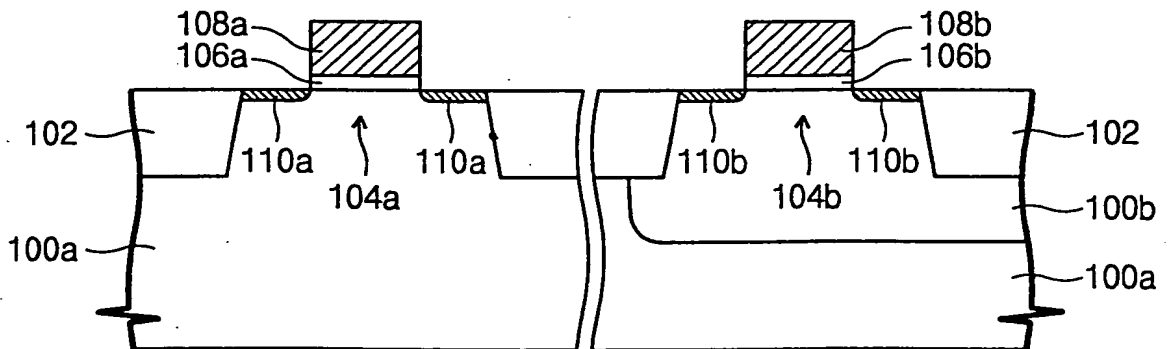
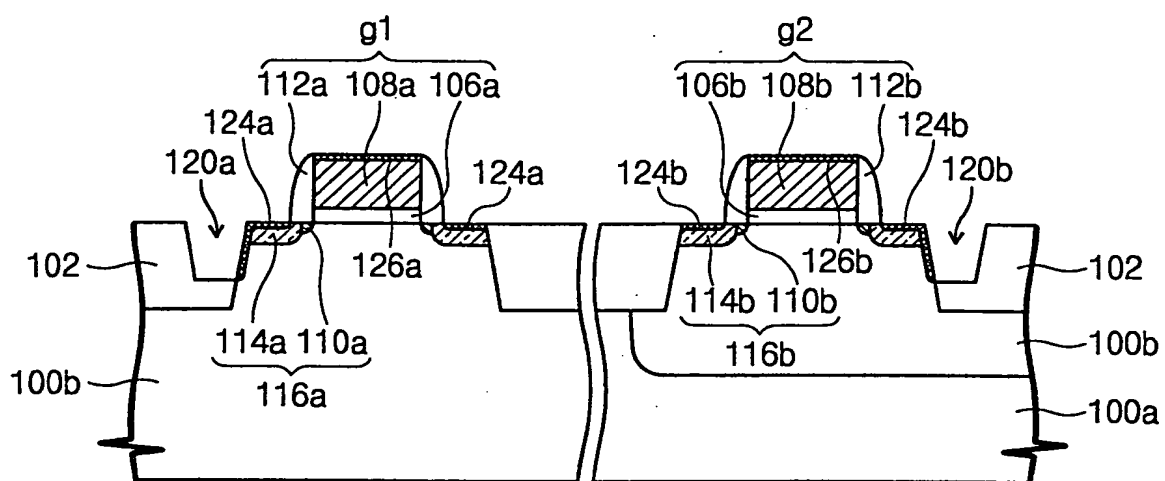


Fig. 5



A cross-sectional view of a semiconductor device, showing two gate regions, g1 and g2, separated by a central channel. The device is built on a substrate 100a. A gate stack 118 is formed on top of the channel and gate regions. The gate stack 118 includes a gate dielectric layer 102 and a gate conductive layer 106. The gate conductive layer 106 is patterned to form gate electrodes 108a and 108b. The gate electrodes 108a and 108b are surrounded by a gate sidewall spacer 112a and 112b. The gate sidewall spacer 112a and 112b are formed on a gate sidewall spacer layer 110a and 110b. The gate sidewall spacer layer 110a and 110b are formed on a gate sidewall spacer layer 114a and 114b. The gate sidewall spacer layer 114a and 114b are formed on a gate sidewall spacer layer 116a and 116b. The gate sidewall spacer layer 116a and 116b are formed on a gate sidewall spacer layer 116b. The gate sidewall spacer layer 116b is formed on a gate sidewall spacer layer 116b. The gate sidewall spacer layer 116b is formed on a gate sidewall spacer layer 116b.

[illegible]



Fi. 6

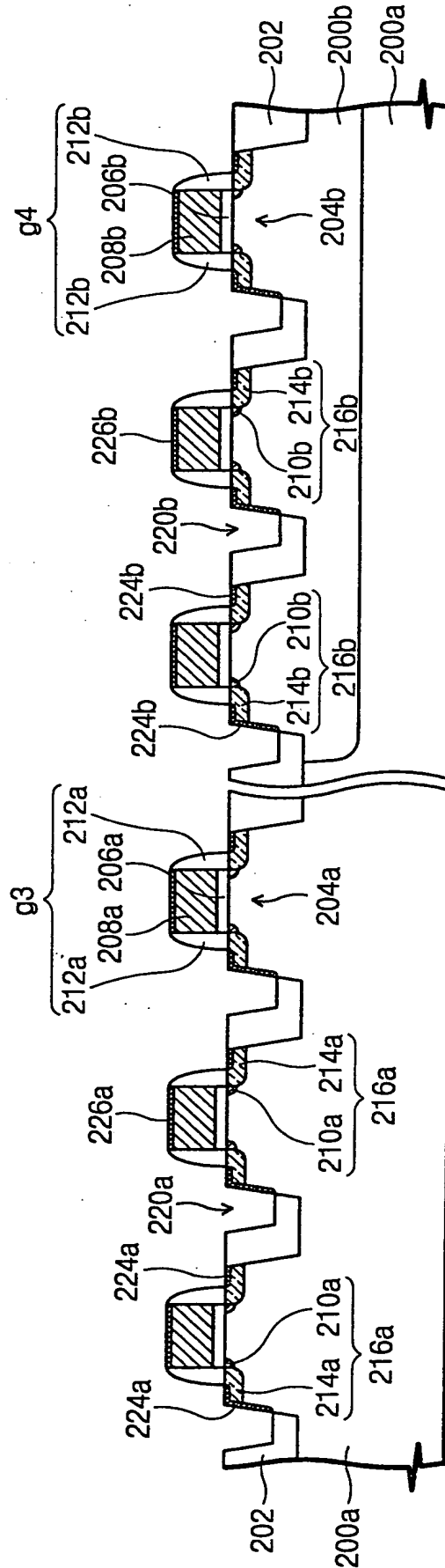


Fig. 10

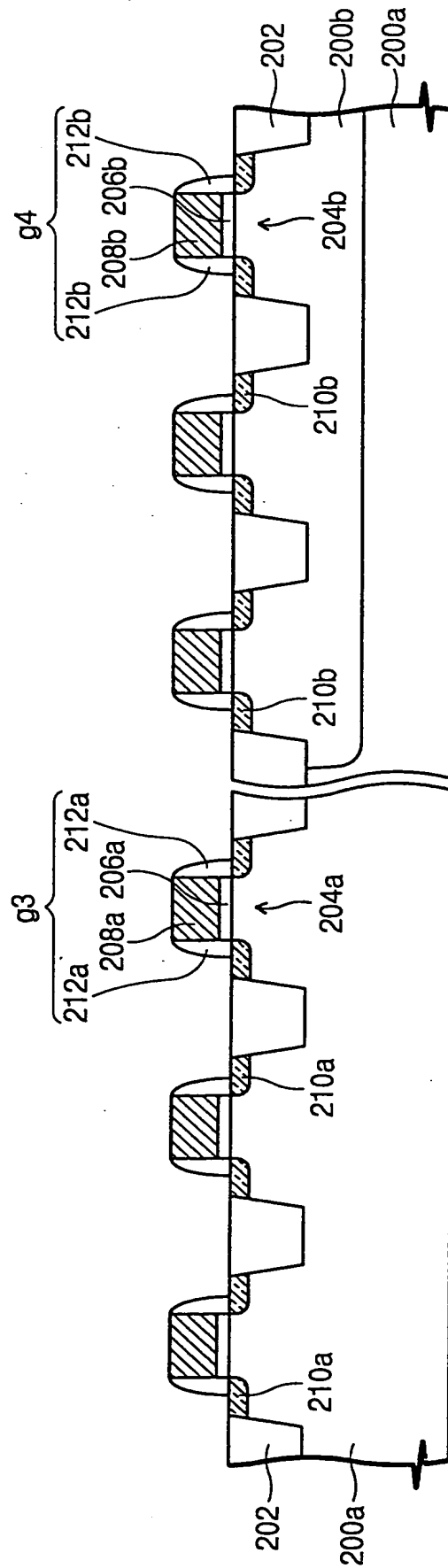


Fig. 11

